

# PATENT SPECIFICATION

(11) 1229946

1229946

## DRAWINGS ATTACHED

- (21) Application No. 51453/68 (22) Filed 30 Oct. 1968  
(31) Convention Application No. 681413 (32) Filed 8 Nov. 1967 in  
(33) United States of America (US)  
(45) Complete Specification published 28 April 1971  
(51) International Classification H 01 L 11/14  
(52) Index at acceptance

H1K 217 21Y 223 22Y 241 277 312 441 474 476 507 511  
51Y 541 54Y 55Y 566 573 576 578 57Y

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## (54) INVERSION LAYER SEMICONDUCTOR DEVICE WITH AZIMUTHALLY DEPENDENT CARRIER MOBILITY

(71) We, TEXAS INSTRUMENTS INCORPORATED, a Corporation organized according to the laws of the State of Delaware, United States of America, of 13500 North Central Expressway, Dallas, Texas, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates generally to semiconductor devices, and more particularly, but not by way of limitation, relates to integrated circuits using inversion layer devices such as metal-insulator-semiconductor field effect transistors.

According to the present invention there is provided a semiconductor device having an essentially two-dimensional conduction layer disposed substantially parallel to a crystallographic plane of a semiconductor crystal which exhibits azimuthally dependent carrier mobility and at least one metal-insulator-semiconductor field effect component on said conduction layer, the or each component having a conduction path including said layer.

Carrier mobility is one of the most important parameters to be considered when designing integrated circuits using inversion layer devices such as the metal-oxide-semiconductor field effect transistors (MOSFET). Although it is generally desirable to have a high carrier mobility for most circuit applications, it is desirable for certain applications to have a low carrier mobility. Others have investigated the carrier mobilities in inversion layers on the various crystallographic planes of silicon crystal identified by the well-known Miller indices. As a result of those investigations, it was heretofore believed that the highest electron mobility occurred in inversion layers disposed parallel to the (100) crystallographic plane and that the highest hole mobility occurs in inversion layers disposed parallel to the (111) plane. For this and other reasons, it has been the accepted practice to fabricate most

MOS field effect devices on the surface of a silicon crystal oriented parallel to the (111) crystallographic plane.

We have discovered that the greatest carrier mobility in a p-type inversion layer in n-type silicon actually exists in the (110) crystallographic plane, and more particularly exists in

the direction perpendicular to the (110) crystallographic plane. Further, we have discovered that the carrier mobility in an inversion layer parallel to the (110) plane is azimuthally dependent, and has a minimum value in a direction perpendicular to the (001) crystallographic plane, which is at right angles to the direction of maximum carrier mobility. Although experimental data is not available at this time to absolutely confirm the fact, theoretical analysis performed in the light of this discovery predicts that substantially any semiconductor crystal, such as germanium, the Group III—Group V, the Group II—Group VI semiconductors, and the tertiary combinations of these elements, will have crystallographic planes in which carrier mobility is azimuthally dependent.

Our discovery has far reaching implications and is particularly useful in fabricating field effect transistors having inversion layers where a high carrier mobility is desired, or where the combination of a high carrier mobility and a low carrier mobility is desired in a single integrated circuit, such as in a common inverter comprised of a driver transistor and a load transistor.

The invention may best be understood by reference to the following detailed description of illustrative embodiments, when read in conjunction with the accompanying drawings, wherein:

FIGURE 1 is a plan view of a Hall bar device used to collect mobility data;

FIGURE 2 is a graph illustrating the carrier mobility with respect to gate voltage in p-type inversion layers formed parallel to various crystallographic planes in silicon and in

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various azimuthal directions within the plane;

FIGURE 3 is a schematic circuit diagram of a typical inverter formed by MOS field effect transistors; and

5 FIGURE 4 is a simplified plan view illustrating how the inverter of FIGURE 3 can be geometrically arranged in an integrated circuit in accordance with a specific aspect of the present invention.

10 The carrier mobility in various azimuthal directions in p-type inversion layers formed at various surfaces of n-type silicon has been determined by fabricating metal-oxide-semiconductor (MOS) transistors in the form of Hall bars on selected surfaces of silicon crystals. The Hall bars were fabricated as shown in FIGURE 1 and comprised boron diffused regions forming the source 2, drain 4 and Hall contact regions 6. The dielectric over the gate region was silicon dioxide thermally grown at 950°C and doped with phosphorus. A metal gate 8 has the shape illustrated and a gate contact 8a. The devices had a width (W) of 0.254 mm and a length (L) of 2.29 mm. The oxide thickness (t) in the area of reduced thickness was nominally 1,000 angstroms. The devices were enhancement mode field effect transistors with threshold voltages  $V_T$  varying from three to six volts.

30 The Hall measurements were made using a magnetic field of 5,000 gauss, although it was determined that the mobility measurements were independent of magnetic field strength up to 6,000 gauss. Although the absolute accuracy of the Hall mobility measurements was estimated at  $\pm 8\%$ , reproducibility was well within these limits. The devices were fabricated on the (110), (100) and (111) planes of silicon, and in various azimuthal directions 35 on each plane, and Hall mobility measurements 40 made on each.

The measured Hall mobility ( $\mu_H$ ) was then converted to conductivity mobility ( $\mu_c$ ) which is deduced from the conductance ( $g_s$ ) of the 45 Hall bar devices shown in FIGURE 1 by the expression

$$g_s = \frac{\mu_c \epsilon_0 \epsilon_{ox} \cdot W}{t \cdot L} (V_g - V_T - V_d) \quad (1)$$

where

$V_g$ =gate voltage

50  $V_T$ =threshold voltage

$V_d$ =drain voltage

$\epsilon_{ox}\epsilon_0$ =dielectric constant of the oxide

t=thickness of the oxide

It was found that the conductivity mobility  $\mu_c$  55 was  $1.25 \pm 0.05$  times the Hall mobility  $\mu_H$  for material having from one to ten ohm-centimeters resistivity in the inversion layer formed on the (110), (100), and (111) planes. This value compares favorably with the 60 theoretical value of 1.13 reported by J. N.

Zemel, in the Physical Review 112, (1958) at page 762. Care was taken to insure that the potential difference between source and drain was small compared with the gate voltage above threshold, thus insuring that the perpendicular electrical field in the inversion layer was uniform over the length of the device.

The conductivity carrier mobility derived by this process is indicated in FIGURE 2. The conductivity mobility of the inversion layer of the Hall device disposed parallel to the (111) crystallographic plane is indicated by curve 10, which is applicable regardless of the azimuthal orientation of current flow. The carrier mobility for inversion layers parallel to the (100) crystallographic plane is represented by curve 12, which is also independent of the azimuthal direction of current flow. The carrier mobility in inversion layers disposed parallel to the (110) crystallographic plane are represented by curves 14 and 16. Curve 14 represents the carrier mobility in a direction

perpendicular to the [110] crystallographic plane, and curve 16 represents the carrier mobility in a direction perpendicular to the (100) crystallographic plane. It will be noted

that the current mobility in the (110) direction is approximately 40% greater than the carrier mobility perpendicular to the (001) crystallographic plane.

The anisotropy of the experimental data shown in FIGURE 1 can be predicted by accepting Neumann's principle that every physical property of a material will have the same symmetry as the crystallographic form of a material. Using Neumann's classical method of studying the effect of symmetry, the symmetry operators constituting the point group of the crystal are successively applied on the tensor representing the physical property. After each symmetry operation on the tensor, it is demanded that the tensor shall remain invariant. Thus, certain conditions governing the relations between the various components of the tensor describing the physical properties emerge, and arising out of these conditions some of the tensor components vanish leaving a given number of nonvanishing and mutually independent constants for a given physical property of a crystal of a certain symmetry.

The most general form of a two-dimensional resistivity tensor as applied to a surface inversion layer is

$$p = \begin{pmatrix} p_{11} & p_{12} \\ p_{21} & p_{22} \end{pmatrix} \quad (2)$$

If there is no anisotropic stress in the inversion layer, the resistivity tensor must contain the symmetry of the crystal in the plane of the layer. For example, silicon is a cubic crystal and so a (100) surface must contain the symmetry of a cross section through the cube

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in this plane, that is a square. The resistivity tensor for a (100) inversion layer must therefore be invariant to certain reflections and 90° rotational operations. Applying these restrictions to the tensor, one deduces that the resistivity (and hence also the mobility) must be isotropic on this plane. If this procedure is repeated for the (111) plane, it is found that isotropic resistivity is again necessary as a result of the crystal symmetry. On the (110) plane, choosing the [001] direction as the principal axis, it is found that the tensor reduces to

$$\begin{pmatrix} p_{11} & 0 \\ 0 & p_{22} \end{pmatrix} \quad (3)$$

which is not isotropic unless this is required by some consideration other than symmetry.

Therefore, although experimental data only for silicon has been compiled to date, anisotropic resistivity can be predicted using this theoretical procedure and can then be measured using the Hall bar approach previously des-

cribed in substantially any semiconductor material.

For many MOSFET applications, the highest possible carrier mobility in the inversion layer is desired. For n-type silicon, the current flow in the essentially two-dimensional current path represented by the relatively thin p-type inversion layer, which may be on the order of 100 angstroms thick, should be in the (110) crystallographic plane and in the

[110] direction.

The azimuthally dependent characteristics of the carrier mobility in semiconductors can be used to advantage in integrated circuits where various circuit components require different carrier mobilities for optimum performance. One example is the fundamental inverter illustrated in FIGURE 3. MOS transistor  $Q_1$  is the active drive device, and MOS transistor  $Q_2$  is the passive load device. Analysis of the circuit when operated at saturated load resistance results in the expressions:

$$\frac{\mu_2 \epsilon \epsilon_0 W_2}{2 t_{ox} L_2} [(V_{ss} - V_o) - V_T]^2 = \frac{\mu_1 \epsilon \epsilon_0 W_1}{2 t_{ox} L_1} [2(V_{in} - V_T)V_o - V_o^2] \quad (4)$$

for  $|V_{in} - V_T| \geq |V_o|$

$$\frac{\mu_2 \epsilon \epsilon_0 W_2}{2 t_{ox} L_2} [(V_{ss} - V_o) - V_T]^2 = \frac{\mu_1 \epsilon \epsilon_0 W_1}{2 t_{ox} L_1} (V_{in} - V_T)^2 \quad (5)$$

for  $|V_{in} - V_T| < |V_o|$

where  $\mu$  is the carrier mobility of the respective devices,  $\epsilon \epsilon_0$  is the dielectric constant of the gate oxide,  $t_{ox}$  is the thickness of the gate oxide,  $W$  is the width of the channel of the respective device,  $L$  is the length of the channel of the respective device, and  $V_T$  is the threshold voltage.

It is frequently desirable to have the impedance of the load transistor  $Q_2$  as high as possible, and the impedance of the drive transistor  $Q_1$  as low as possible. Since the mobility values  $\mu_1$  and  $\mu_2$  were heretofore thought to be equal, the impedance ratios have heretofore been adjusted by selecting the channel width  $W$  and the channel length  $L$  of the driver and load devices. For example, to achieve high impedance in the channel of the load transistor  $Q_2$ , the channel length  $L_2$  of the device must be lengthened. Conversely, to achieve the desired low impedance for the drive transistor  $Q_1$ , the channel length  $L_1$  is made as short as possible.

In accordance with the present invention, the components of the inverter of FIGURE 3 are laid out as shown in FIGURE 4 on the (110) surface of a slice of n-type silicon 18

so that the driver transistor  $Q_1$  has a maximum mobility and the load transistor  $Q_2$  has a minimum mobility. Transistor  $Q_1$  is formed by diffused source and drain regions 20 and 22. A relatively thick layer 24 of silicon dioxide is formed over the surface of the silicon slice, but has a thin region 26, typically about 1,000 angstroms thick, over the channel between the source and drain regions. A metal film 28 extends over the thin layer of oxide in region 26 to form the metal gate. A metal film 30 is in direct ohmic contact with the diffused source region 20 through an opening 30 in the oxide layer 24. The load transistor  $Q_2$  is formed in the same manner by a diffused source region 32, which is a continuation of drain region 22, diffused drain region 34, and metal gate 36 which is disposed over a region 38 of thin oxide. The gate 36 is shorted to the drain region 34 through an opening 40 in the oxide, and  $V_{ss}$  and  $V_{dd}$  are the same value. The output voltage  $V_o$  is then through metal film 42 which is in ohmic contact with the diffused regions 22-32 through an opening 44 in the oxide layer.

The source and drain diffusions 20 and 22

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of the driver transistor  $Q_1$  are arranged such that current flow through the inverted layer forming the channel is in the [110] direction, that is in a direction normal to the (110) crystallographic plane. This provides a maximum mobility value for  $\mu_3$  as can be seen from the data presented in FIGURE 1. The source and drain diffusions 32 and 34 of the load transistor  $Q_2$  are disposed such that current flow through the inversion layer forming the channel is in a direction at right angles to the direction of current flow through the channel of transistor  $Q_1$ , which is in the (001) direction, i.e., normal to the (001) crystallographic plane, so that the carrier mobility value  $\mu_2$  for the load transistor will be a minimum value. As a result of this procedure, the ratio of the impedance of the load transistor to the impedance of the driver transistor can be increased for a given geometric size in order to improve performance, or conversely, the geometric length of the load transistor can be reduced for a given impedance ratio, thus resulting in a significant saving of area on the integrated circuit.

Although a specific example has been shown which utilizes the azimuthally dependent carrier mobility of a particular plane in a semiconductor, it will be appreciated that the same concept is applicable to any circuit or subcircuit in which it is desirable to use a variable carrier mobility. This design capability is enhanced by the fact that the carrier mobility for the azimuthal directions between the maximum values normal to the (110) plane and the minimum values normal to the (001) plane are intermediate values which are dependent upon the particular azimuthal direction. Thus the design engineer can select substantially any carrier mobility between the maximum and minimum merely by the proper geometric orientation of the source and drain diffusions for the device. Also, while the specific embodiment of the concept described herein is a p-type inversion layer formed in n-type silicon, the principle is applicable to any thin layer which behaves essentially as a two-dimensional conduction sheet in any plane of any semiconductor which exhibits azimuthally dependent carrier mobility.

#### WHAT WE CLAIM IS:—

1. A semiconductor device having an essentially two-dimensional conduction layer disposed substantially parallel to a crystallographic plane of a semiconductor crystal which exhibits azimuthally dependent carrier mobility and at least one metal-insulator-semiconductor field effect component on said conduction layer, the or each component having a conduction path including said layer.
2. A device according to Claim 1 wherein

the semiconductor is silicon and the conduction layer is disposed substantially on the (110) plane.

3. A device according to Claim 2 wherein the current flow of the component or at least one of said components through its conduction

path is substantially perpendicular to the (110) crystallographic plane to obtain maximum carrier mobility.

4. A device according to Claim 2 or 3 wherein the current flow of the component or at least one of said components through its conduction path is substantially perpendicular to the (001) crystallographic plane to obtain minimum carrier mobility.

5. A device according to Claim 1 wherein there are at least two components on said conduction layer, the current flow of one of said components through its conduction path is in the maximum carrier mobility direction and the current flow of another of said components through its conduction path is in the direction of minimum carrier mobility.

6. A semiconductor device which comprises a slice of semiconductor material having a pair of metal-insulator-semiconductor transistors formed on a surface of the slice disposed parallel to a crystallographic plane which exhibits azimuthally dependent carrier mobility, the transistors being geometrically oriented such that the direction of current flow in one transistor is in a different azimuthal direction from the direction of current flow in the other transistor whereby the effective carrier mobilities in the two transistors are different.

7. A device according to Claim 6 wherein one transistor of the pair is a driver and the other transistor is a load, and the driver transistor is oriented such that current flow through it is in the azimuthal direction of greatest carrier mobility and the load transistor is oriented such that current flow through it is in the azimuthal direction of lowest carrier mobility.

8. A device according to Claim 7 wherein the semiconductor is silicon and the surface of the slice is parallel to the (110) crystallographic plane.

9. A device according to Claim 8 wherein current through the driver transistor is in a direction substantially normal to the (110) crystallographic plane and current through the load transistor is in a direction substantially normal to the (001) crystallographic plane.

10. A device according to Claim 6 wherein the semiconductor is silicon and the surface of the slice is disposed parallel to the (110) crystallographic plane.

11. An integrated circuit comprising a plurality of metal-insulator-semiconductor transistors formed on the surface of a single semiconductor crystal, the surface being disposed substantially parallel to a crystallographic plane which exhibits azimuthally

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- dependent carrier mobility in a thin inversion layer at the surface.
12. A semiconductor device comprising a metal-insulator-semiconductor transistor having a thin inversion layer formed on the (110) crystallographic plane of a silicon crystal with current flowing through the inversion layer in a direction normal to the (110) crystallographic plane. 15
- 5 10 13. A semiconductor device comprising a metal-insulator-semiconductor transistor having a thin inversion layer formed on the (110) crystallographic plane. 20
14. An integrated circuit substantially as herein described with reference to figure 4 of the accompanying drawings.

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Printed for Her Majesty's Stationery Office, by the Courier Press, Leamington Spa, 1971.  
Published by The Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from  
which copies may be obtained.

1229946

## COMPLETE SPECIFICATION

1 SHEET

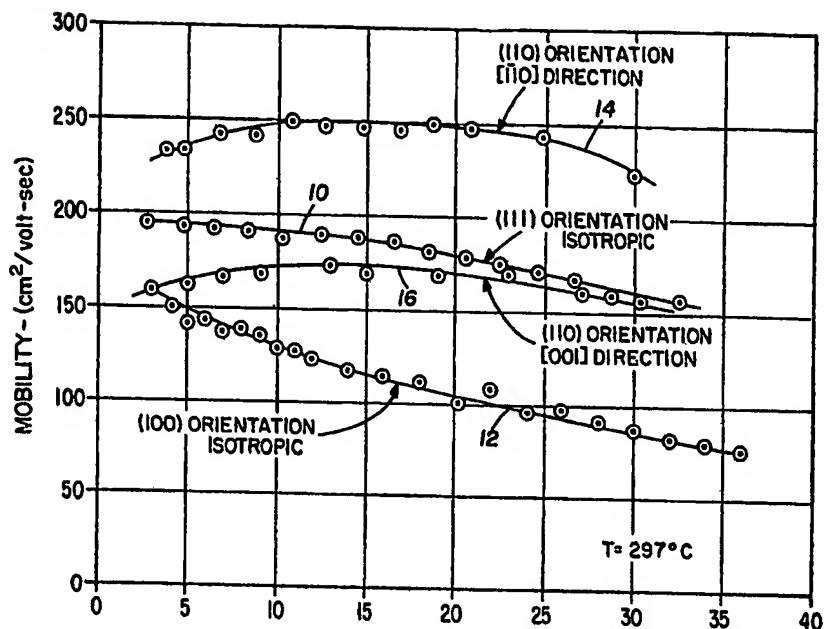
*This drawing is a reproduction of  
the Original on a reduced scale*

FIG. 2

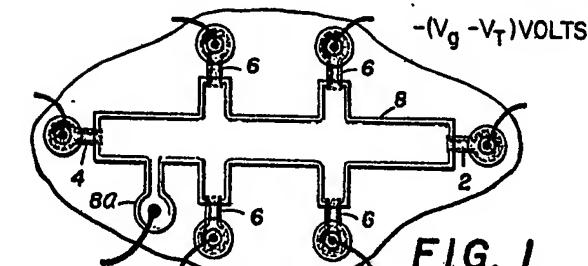


FIG. 1

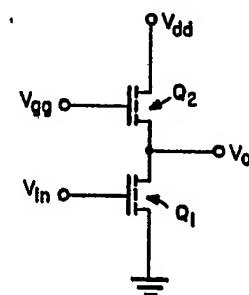


FIG. 3

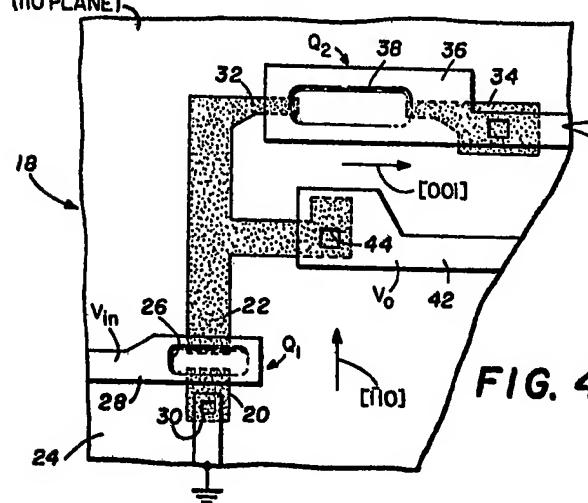


FIG. 4